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EXAMINER	
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ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/980,098	ITAMI, SHINJI	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,6,8 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,6,8 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the After Final Amendment filed on 28th of February 2006. Claims 1, 5, 6, 8, 10, and 12 have been amended; no claim has been canceled; and claim 14 has been newly added since the RCE Final Office Action was mailed on 28th of November 2005.

2. Receipt is acknowledged of the request filed on 28th of March 2006 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/980,098, which the request is acceptable and an RCE has been established. Currently, claims 1, 3, 5, 6, 8, and 10-14 are pending in this Application.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 6 and 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

In fact, the claims 6 and 8 recite the limitation "when a waveform is deformed by the trigger signal during the data transmission/reception, the memory start address is not incremented" in lines 16-17 of the claim 6, and in lines 19-20 of the claim 8, respectively. However, the claimed limitation was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application

was filed, had possession of the claimed invention. In other words, the original specification does not disclose that the claimed subject matter "trigger signal" could deform the claimed subject matter "waveform".

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim 14 recites the limitation "the address" in line 2. However, its prior claim 1 recites the claimed subject matter "an address" in line 8, and this claim 14 recites a different claimed subject matter "an address" in line 2, as well. Therefore, the recited subject matter "the address" in line 2 of the claim 14 fails to clearly point out which one of the two different subject matters "address" in line 8 of the claim 1 or in line 2 of the claim 14 is the antecedent basis of the subject matter "the address" in line 2 of the claim 14, and then it makes the claim 14 be indefinite.

The Examiner presumes that the term “an address” in line 2 of the claim 14 could be considered as --an external address-- in light of the specification since it is not clearly pointed out in the claims.

Claim Objections

7. Claim 14 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form.

Actually, the claim 14 recites the limitation " the address is transmitted only in the address bus" in line 2. However, the scope of the claimed invention is limited in its prior claim 1 such that the data transmission path employs a **same signal line** as **an address bus** and **a data bus** mutually (See claim 1, lines 5-6). Therefore, the address cannot be transmitted only in the address bus, but be transmitted in a same signal line as an address bus and a data bus mutually.

The Examiner presumes that the term "an address bus" in line 2 of the claim 14 could be considered as --an internal address bus-- in light of the specification for the purpose of claim rejection based on prior art.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3, 6, 8, and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter AAPA] in view of Appelbaum et al. [US 5,758,188 A; hereinafter Appelbaum].

Referring to claim 1, AAPA discloses a data transmission system (Fig. 16), comprising:

- a primary board (i.e., primary board 100 of Fig. 16);
- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and
- a data transmission path (i.e., data transmission bus 300 of Fig. 16) carrying out data transmission/reception (See page 1, lines 16-20) between the primary board (i.e., said

primary board on the transmission transmitter side) and the secondary boards (i.e., said secondary boards on the transmission receiver side),

- the data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 19 and page 2, lines 11-15),
  - wherein when the data access (i.e., Reading Process in Fig. 20) is executed from the primary board to the secondary boards (See Figs. 20 and 21), informing a start address (i.e., Step S211- A15:2/D15:0 START ADDRESS OUTPUT in Fig. 20) required for data access (See page 3, line 24 through page 4, line 4), and
  - wherein an address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20) used in the data access (i.e., accessing DATA 1-4 in Fig. 19) in the secondary boards (i.e., said DATA 1-4 are in said secondary boards being addressed by said generated address; See page 4, lines 8-21) is generated based on the start address (i.e., said A15:2/D 15:0 START ADDRESS OUTPUT), a predetermined trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 19) and a cycle signal (i.e., signal A1:0 (205) in Figs. 19 and 20) indicating switching of data (See page 5, lines 6-18), the cycle signal is combined with the trigger signal (i.e., said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 4, line 22 through page 5, line 18), and

- wherein the cycle signal (i.e., said signal A1:0 (205)) counts plural times of a leading edge of a clock signal of the primary board (i.e., each sequence 0h, 1h, 2h and 3h of said signal A1:0 (205) taking one or more TRG201 T signals inherently shows said signal A1:0 (205) counts plural times of a leading edge of a clock signal of the primary board in Fig. 19).

AAPA does not teach that the cycle signal counts plural times of the leading edge of the clock signal of the primary board prior to toggle of the cycle signal.

Appelbaum discloses a synchronous DMA burst transfer protocol (See Abstract), wherein

- a cycle signal (i.e., Strobe in Fig. 2) counts plural times of a leading edge of a clock signal (i.e., time t_0, t_1, t_2, t_3, t_4 in Fig. 2) of a primary board (i.e., Host 35 of Fig. 2) prior to toggle of the cycle signal (See col. 4, lines 41-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said cycle signal (i.e., signal A1:0 (205)), as disclosed by AAPA, by said cycle signal (i.e., Strobe) with said synchronous DMA burst transfer protocol, as disclosed by Appelbaum, for the advantage of providing a significantly increased data transfer rate between said primary board (i.e., host device) and said secondary board (i.e., peripheral drive device) and being operable within existing data transmission path architecture (i.e., bus system architecture; See Appelbaum, col. 4, line 66 through col. 5, line 6).

Referring to claim 3, AAPA teaches

- when the address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20) is generated based on the trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 19; See page 4, line 22 through page 5, line 5), the address is generated sequentially by incrementing the start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 19) in response to a

timing of the trigger signal (See trigger signal TRG201 and signal A1:0 (205) in Figs. 17 and 19, and page 5, lines 6-18).

Referring to claim 6, AAPA discloses a method of transmitting data by a data transmission system (See page 1, line 14 through page 2, line 2 and Fig. 16) comprising a primary board (i.e., primary board 100 of Fig. 16), secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16), and a data transmission path (i.e., data transmission bus 300 of Fig. 16) for carrying out data read (See page 1, lines 16-20 and page 3, lines 14+) between the primary board (i.e., said primary board on the transmission transmitter side) and the secondary boards (i.e., said secondary boards on the transmission receiver side), wherein the data transmission path (i.e., said data transmission bus) employs a same signal line (i.e., A15:2/D15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 19 and page 2, lines 11-15), the method comprising:

- informing a trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 19) combined with a cycle signal (i.e., signal A1:0 in Fig. 19; in fact, said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 3, line 24 through page 4, line 4) indicating a timing of data access (See page 4, line 22 through page 5, line 20), and a start address (i.e., Step S211- A15:2/D15:0 START ADDRESS OUTPUT in Fig. 20) required for data read (i.e., data reading in Figs. 20 and 21) via the data transmission path (i.e., data transmission bus);
- switching the data transmission path to which the start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 19);
- accessing a memory (i.e., Memory 208 of Fig. 17) based on the start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 19 and Steps of S211 and S214

in Fig. 20) and sending out a read result onto the data transmission path (See page 5, lines 4-5); and

- incrementing the start address (i.e., said Start Address being incremented with A1:0 (205) in sequence of 0h, 1h, 2h and 3h in Fig. 19), and then sending out a read result onto the data transmission path by accessing the memory based on the incremented address (See timing diagram in Fig. 19 and page 5, lines 8-20),
    - wherein the start address is not incremented when a waveform is deformed by the trigger signal during the data read (See Fig. 21, in fact, an address generation at Step S233 is not repeated (i.e., going to End of Reading Process at Step S232) for address increment when a waveform of FRAME is not L (i.e., Low) caused by signal deformation to H (i.e., High) in the middle of data accessing process by trigger signal TRG, e.g., a noisy trigger signal, inherently anticipates that said start address is not incremented when a waveform is deformed by said trigger signal during said data read. In other words, a synthesized address construction, which is based on Start Address A15:2/D15:0 (206) with signal A1:0 (205), is not repeated, viz., no address increment, when a waveform of FRAME 202 is deformed to H (i.e., High) in the middle of data accessing process by a noise from trigger signal TRG201, for example, in Fig. 19), and
    - wherein the secondary board does not shift to a next process until the cycle signal (i.e., signal A0 of said signal A1:0) has been toggled (See page 4, lines 8-21; i.e., the secondary board does not proceed to the next process S234 Memory Read in Fig. 21 until the bus direction has been changed from input to output, and the cycle has been switched from the address cycle to the data reading

cycle), and leading and trailing edges of the trigger signal are detected in combination with detecting the toggle states of the cycle signal (See page 4, line 15 through page 5, line 3),

- wherein the cycle signal (i.e., said signal A1:0 (205)) counts plural times of a leading edge of a clock signal of the primary board (i.e., each sequence 0h, 1h, 2h and 3h of said signal A1:0 (205) taking one or more TRG201 T signals inherently shows said signal A1:0 (205) counts plural times of a leading edge of a clock signal of the primary board in Fig. 19).

AAPA does not teach that the cycle signal counts plural times of the leading edge of the clock signal of the primary board prior to toggle of the cycle signal.

Appelbaum discloses a synchronous DMA burst transfer protocol (See Abstract), wherein

- a cycle signal (i.e., Strobe in Fig. 2) counts plural times of a leading edge of a clock signal (i.e., time t_0, t_1, t_2, t_3, t_4 in Fig. 2) of a primary board (i.e., Host 35 of Fig. 2) prior to toggle of the cycle signal (See col. 4, lines 41-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said cycle signal (i.e., signal A1:0 (205)), as disclosed by AAPA, by said cycle signal (i.e., Strobe) with said synchronous DMA burst transfer protocol, as disclosed by Appelbaum, for the advantage of providing a significantly increased data transfer rate between said primary board (i.e., host device) and said secondary board (i.e., peripheral drive device) and being operable within existing data transmission path architecture (i.e., bus system architecture; See Appelbaum, col. 4, line 66 through col. 5, line 6).

Referring to claim 8, AAPA discloses a data transmission system (Fig. 16) comprising:

- a primary board (i.e., primary board 100 of Fig. 16);

- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and
- a data transmission path (i.e., data transmission bus 300 of Fig. 16) for carrying out data write (See page 1, lines 16-20 and page 5, lines 21+) between the primary board (i.e., said primary board on the transmission transmitter side) and the secondary boards (i.e., said secondary boards on the transmission receiver side), where the data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 22) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 22 and page 2, lines 11-15), wherein
    - the carrying out of the data write (i.e., --Writing Process-- on page 5) is executed by:
        - informing a trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 22) combined with a cycle signal (i.e., signal A1:0 in Fig. 22; in fact, said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 6, lines 17-24) indicating a timing of data access (See page 6, line 25 through page 7, line 11) and a start address (i.e., Step S241- A15:2/D15:0 START ADDRESS OUTPUT in Fig. 23) required for data write (i.e., data writing in Figs. 23 and 24) via the data transmission path (i.e., said data transmission bus),
        - switching the data transmission path to which the start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 22), and then sending out a predetermined data (i.e., Data 1 in step S242 in Fig. 23) to be written to a memory (i.e., Memory 208 of Fig. 17);

- accessing the memory (i.e., Memory) based on the start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 22 and Steps of S241 and S242 in Fig. 23), and then writing the predetermined data to be written into the memory (See page 6, lines 6-16),
- incrementing the start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 22), and then writing sequentially the predetermined data (i.e., Data 2-4 in steps S244, S246 and S248 in Fig. 23), that are sent out via the data transmission path (i.e., Data Bus), into the memory by accessing the memory based on the incremented address (See timing diagram in Fig. 22 and page 6, line 17 through page 7, line 6),
- detecting leading and trailing edges of the trigger signal in combination with detecting toggle states of the cycle signal (i.e., detecting TRG with detecting toggle states of Addressing cycle phase and Data cycle phase in Fig. 22; See page 6, line 17 through page 7, line 1),
- not incrementing the start address when a waveform is deformed by the trigger signal during the data write (See Fig. 24, in fact, an address generation at Step S262 is not repeated (i.e., going to End of Writing Process at Step S261) for address increment when a waveform of FRAME is not L (i.e., Low) caused by signal deformation to H (i.e., High) in the middle of data writing process by trigger signal TRG, e.g., a noisy trigger signal, inherently anticipates that said address is not incremented when a waveform is deformed by said trigger signal. In other words, a synthesized address construction, which is based on Start Address

A15:2/D15:0 (206) with signal A1:0 (205), is not repeated, viz., no address increment, when a waveform of FRAME 202 is deformed to H (i.e., High) in the middle of data writing process by a noise from trigger signal TRG201, for example, in Fig. 22), and

- not shifting the secondary board to a next process until the cycle signal has been toggled (See page 6, lines 15-24; i.e., the secondary board does not proceed to the next process S264 Memory Write in Fig. 24 until the cycle has been switched from the address cycle to the data reading cycle),
  - wherein the cycle signal (i.e., said signal A1:0 (205)) counts plural times of a leading edge of a clock signal of the primary board (i.e., each sequence 0h, 1h, 2h and 3h of said signal A1:0 (205) taking one or more TRG201 T signals inherently shows said signal A1:0 (205) counts plural times of a leading edge of a clock signal of the primary board in Fig. 19).

AAPA does not teach that the cycle signal counts plural times of the leading edge of the clock signal of the primary board prior to toggle of the cycle signal.

Appelbaum discloses a synchronous DMA burst transfer protocol (See Abstract), wherein

- a cycle signal (i.e., Strobe in Fig. 2) counts plural times of a leading edge of a clock signal (i.e., time t_0, t_1, t_2, t_3, t_4 in Fig. 2) of a primary board (i.e., Host 35 of Fig. 2) prior to toggle of the cycle signal (See col. 4, lines 41-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said cycle signal (i.e., signal A1:0 (205)), as disclosed by AAPA, by said cycle signal (i.e., Strobe) with said synchronous DMA burst transfer protocol, as

disclosed by Appelbaum, for the advantage of providing a significantly increased data transfer rate between said primary board (i.e., host device) and said secondary board (i.e., peripheral drive device) and being operable within existing data transmission path architecture (i.e., bus system architecture; See Appelbaum, col. 4, line 66 through col. 5, line 6).

Referring to claim 10, AAPA discloses a method for carrying out data write (See page 1, lines 16-20 and page 5, lines 21+) between a primary board (i.e., primary board 100 of Fig. 16 on the transmission transmitter side) and secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16 on the transmission receiver side) by using a data transmission path (i.e., data transmission bus 300 of Fig. 16), which employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 22) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 22 and page 2, lines 11-15), comprising:

- informing a trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 22) combined with a cycle signal (i.e., signal A1:0 in Fig. 22; in fact, said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 6, lines 17-24) indicating a timing of data access (See page 6, line 25 through page 7, line 11) and a start address (i.e., Step S241-A15:2/D15:0 START ADDRESS OUTPUT in Fig. 23) required for data write (i.e., data writing in Figs. 23 and 24) via the data transmission path (i.e., data transmission bus);
- switching the data transmission path to which the start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 22), and then sending out a predetermined data (i.e., Data 1 in step S242 in Fig. 23) to be written to a memory (i.e., Memory 208 of Fig. 17);

- accessing the memory (i.e., Memory) based on the start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 22 and Steps of S241 and S242 in Fig. 23), and then writing the predetermined data to be written into the memory (See page 6, lines 6-16);
- incrementing the start address (i.e., said Start Address being incremented with A1:0 (205) in sequence of 0h, 1h, 2h and 3h in Fig. 22), and then writing sequentially the predetermined data (i.e., Data 2-4 in steps S244, S246 and S248 in Fig. 23), that are sent out via the data transmission path (i.e., Data Bus), into the memory by accessing the memory based on the incremented address (See timing diagram in Fig. 22 and page 6, line 17 through page 7, line 6),
    - wherein the cycle signal (i.e., said signal A1:0 (205)) counts plural times of a leading edge of a clock signal of the primary board (i.e., each sequence 0h, 1h, 2h and 3h of said signal A1:0 (205) taking one or more TRG201 T signals inherently shows said signal A1:0 (205) counts plural times of a leading edge of a clock signal of the primary board in Fig. 19).

AAPA does not teach that the cycle signal counts plural times of the leading edge of the clock signal of the primary board prior to toggle of the cycle signal.

Appelbaum discloses a synchronous DMA burst transfer protocol (See Abstract), wherein

- a cycle signal (i.e., Strobe in Fig. 2) counts plural times of a leading edge of a clock signal (i.e., time t_0, t_1, t_2, t_3, t_4 in Fig. 2) of a primary board (i.e., Host 35 of Fig. 2) prior to toggle of the cycle signal (See col. 4, lines 41-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said cycle signal (i.e., signal A1:0 (205)), as disclosed by AAPA, by said cycle signal (i.e., Strobe) with said synchronous DMA burst transfer protocol, as

disclosed by Appelbaum, for the advantage of providing a significantly increased data transfer rate between said primary board (i.e., host device) and said secondary board (i.e., peripheral drive device) and being operable within existing data transmission path architecture (i.e., bus system architecture; See Appelbaum, col. 4, line 66 through col. 5, line 6).

Referring to claim 11, Appelbaum teaches

- the cycle signal (i.e., Strobe in Fig. 2) only indicates the switching of the data (See col. 4, lines 50-58).

Referring to claim 12, AAPA, as modified by Appelbaum, teaches

- the cycle signal (i.e., Strobe in Fig. 2; Appelbaum) is a separate toggle signal having only two states (i.e., separate toggling signal from Data bus having high state and low state in Fig. 2; See Appelbaum, col. 4, lines 50-55) and
    - wherein the trigger signal (i.e., trigger signal TRG201 in Fig. 17; AAPA) illustrates write and read timing of the data transmission path (i.e., data transmission bus 300 of Fig. 16; See page 2, lines 4-6).

Referring to claim 13, AAPA teaches

- the secondary board (i.e., secondary boards A-C 200a-c in Fig. 16) generates (i.e., synthesizes) subsequent addresses used in data access based on the start address (See page 4, line 22 through page 5, line 5) and
    - wherein the subsequent addresses (i.e., continuous memory read addresses) are generated by the secondary board (i.e., being synthesized by said second board at step S233 in Fig. 21) by incrementing last address used (i.e., in fact that

DATA1, DATA2, DATA3, and DATA4 are addressed using Starting address ADDRESS on A15:2/D15:0 (206) and incremental data on A1:0 (205) after being synthesized by said second board in Fig. 19).

Referring to claim 14, AAPA, as modified by Appelbaum, teaches

- the cycle signal (i.e., Strobe in Fig. 2; Appelbaum) is not a portion of an external address (i.e., said Strobe signal is not a part of Addr0-2 in ATA bus 34 of Fig. 2; Appelbaum) and
    - wherein the address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20; AAPA) is transmitted only in an internal address bus (i.e., MA 15:0(209) in Fig. 17; AAPA).

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Appelbaum [US 5,758,188 A] and Kerstein et al. [US 6,021,478 A; Kerstein].

Referring to claim 5, AAPA discloses a data transmission system (Fig. 16) comprising:

- a primary board (i.e., primary board 100 of Fig. 16);
- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and
- a data transmission path (i.e., data transmission bus 300 of Fig. 16) for carrying out data transmission/reception (See page 1, lines 16-20) between the primary board (i.e., said primary board on the transmission transmitter side) and the secondary boards (i.e., said secondary boards on the transmission receiver side), where
    - the data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 19 and page 2, lines 11-15),

- wherein: when the data access (i.e., Reading Process in Fig. 20) is executed from the primary board to the secondary boards (See Figs. 20 and 21), informing a memory start address (i.e., Step S211- A15:2/D 15:0 START ADDRESS OUTPUT in Fig. 20) of the secondary boards required for data access (See page 3, line 24 through page 4, line 4),
- judging in the secondary boards is performing whether or not the memory start address is directed to own station (See page 2, line 25 through page 3, line 3; i.e., Separator 207 in Secondary Board 200 in Fig. 17 is performing the step S201 in Fig. 18), and then executing the data transmission via the data transmission path (i.e., said data transmission bus) by accessing a memory (i.e., Memory 208 of Fig. 17) in own station (i.e., target Secondary Board 200 of Fig. 17) based on the memory start address when the memory start address is directed to own station (See page 3, lines 4-13 and Fig. 18), and
- an address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20) is generated, to which the data transmission is subsequently executed (i.e., steps of S214-S220 in Fig. 20), in the secondary boards (i.e., address is constructed in said secondary boards by synthesizing the address A15:2/D15:0 assigned from said primary board; See page 4, line 24 through page 5, line 2) by incrementing the memory start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 19) after the data transmission based on the memory start address is ended (i.e., steps of S211 and S212 in Fig. 20), and then executing the data transmission via

the data transmission path by accessing the memory of own station (i.e., target Secondary Board) based on the generated address (See timing diagram in Fig. 19 and page 5, lines 6-18),

- wherein a cycle signal (i.e., signal A1:0 in Fig. 20) indicating switching of data (See page 5, lines 6-18) is used in combination with a trigger signal (i.e., said secondary board interprets said signal A1:0 and trigger signal TRG201 in Figs. 17 and 19 as combined for outputting said DATA 1-4; See page 4, line 22 through page 5, line 18), and
- wherein the secondary board does not shift to a next process until the cycle signal (i.e., signal A0 of said signal A1:0) has been toggled (See page 4, lines 8-21; i.e., the secondary board does not proceed to the next process S234 Memory Read in Fig. 21 until the bus direction has been changed from input to output, and the cycle has been switched from the address cycle to the data reading cycle), and leading and trailing edges of the trigger signal are detected in combination with detecting the toggle states of the cycle signal (See page 4, line 15 through page 5, line 3),
- wherein the cycle signal (i.e., said signal A1:0 (205)) counts plural times of a leading edge of a clock signal of the primary board (i.e., each sequence 0h, 1h, 2h and 3h of said signal A1:0 (205) taking one or more TRG201 T signals inherently shows said signal A1:0 (205) counts plural times of a leading edge of a clock signal of the primary board in Fig. 19).

AAPA does not teach that the cycle signal counts plural times of the leading edge of the clock signal of the primary board prior to toggle of the cycle signal.

Appelbaum discloses a synchronous DMA burst transfer protocol (See Abstract), wherein

- a cycle signal (i.e., Strobe in Fig. 2) counts plural times of a leading edge of a clock signal (i.e., time t_0, t_1, t_2, t_3, t_4 in Fig. 2) of a primary board (i.e., Host 35 of Fig. 2) prior to toggle of the cycle signal (See col. 4, lines 41-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said cycle signal (i.e., signal A1:0 (205)), as disclosed by AAPA, by said cycle signal (i.e., Strobe) with said synchronous DMA burst transfer protocol, as disclosed by Appelbaum, for the advantage of providing a significantly increased data transfer rate between said primary board (i.e., host device) and said secondary board (i.e., peripheral drive device) and being operable within existing data transmission path architecture (i.e., bus system architecture; See Appelbaum, col. 4, line 66 through col. 5, line 6).

AAPA, as modified by Appelbaum, does not teach when disturbances are generated on the trigger signal during the data transmission/reception, the memory start address is not incremented.

Kerstein discloses a burst memory transferring (See Abstract), wherein

- a primary board (i.e., CPU 50 of Fig. 5);
- a secondary board (i.e., Burst Memory 51 of Fig. 5);
- a data transmission path (i.e., Address Bus, Data Bus, CE and OE controls in Fig. 5) for carrying out transmission/reception between the primary board and the secondary board (See col. 2, line 66 through col. 3, line 3);
- wherein a burst transfer control including
    - when disturbances are generated on a trigger signal (i.e., OE signal in Fig. 5) during a data transmission/ reception (i.e., when an output disabling signal is generated on said OE signal; in other words, when CPU disturbs memory latch in Step 704 and 705 in Fig. 7), a memory start address is not incremented (i.e.,

suspending memory bursting operation 706 in Fig. 7; See Fig. 6 and col. 2, lines 18-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said burst transfer control, as disclosed by Kerstein, in said data transmission system, as disclosed by AAPA, as modified by Appelbaum, so as to control bursting of data using the trigger signal (i.e., OE signal) without requiring the use of dedicated burst pins for the advantage of reducing design cost and logic complexity by eliminating said dedicated burst pins (See Kerstein, col. 2, lines 32-41).

Response to Arguments

11. Applicant's arguments filed on 28th of February 2006 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "... Claims 5, 6, and 8 have been amended to recite: ..." in the Response page 9, line 14 through page 10, line 19, the Examiner respectfully disagrees.

In contrary to the Applicant's statement, the claims 6 and 8 have not been amended, and thus the claims 6 and 8 are rejected under 35 U.S.C. § 112, first paragraph (See paragraph 4 of the instant Office Action). Instead, only the amended claims 5 and 12 have overcome the claim rejection under 35 U.S.C. § 112, first paragraph. However, the Applicant's arguments with respect to claims 5 and 12 rejections under 35 U.S.C. § 112 are moot in view of the new ground(s) of rejection.

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Dependent claim 13 recites: ... S233 in Fig. 21 of the APA only discloses assigning to the MA 15:0 the transmitted A15:2 and

A1:0. That is, the address MA 15:0 is synthesized from the addresses A 15:2 and A 1:0 ... In the APA, a subsequent address is not generated. In the APA, the address is simply synthesized from the two transmitted addresses ..." in the Response page 1, lines 10-20, the Examiner respectfully disagrees.

According to the Merriam-Webster's Collegiate® Dictionary (10th ed.), the term "synthesize"$_{vb}$ is defined as "produce by synthesis," which means "generate by synthesis." Therefore, in contrary to the Applicant's assertion, the limitations in the claim 13 is clearly taught by AAPA (See page 15, line 18 through page 16, line 3 in the instant Office Action), and thus, the Applicant's argument on this point is not persuasive.

12. Applicant's arguments with respect to claims 1, 5, and 12 have been considered but are moot in view of the new ground(s) of rejection.

In fact, the Applicant argues with the new issue being drawn to the limitations "the cycle signal counts plural times a leading edge of a clock signal of the primary board prior to toggle of the cycle signal" and "when disturbances are generated on the trigger signal during the data transmission/reception, the memory start address is not incremented," which had not been considered in the prior Office Action, and thus, the Applicant's argument on this point is moot in view of further consideration requirement.

Actually, the Examiner brought Appelbaum and Kerstein references in the rejection for the limitations which are not provided by AAPA and all of the other art cited (See *Claim Rejections - 35 USC § 103*).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Vavreck et al. [US 5,402,453 A] disclose apparatus and method for reliably clocking a signal with arbitrary phase.

Herbert [US 6,033,441 A] discloses method and apparatus for synchronizing data transfer.

Zhao et al. [US 6,341,326 B1] disclose method and apparatus for data capture using latches, delays, parallelism, and synchronization.

Anand [US 6,581,124 B1] discloses high performance internal bus for promoting design reuse in north bridge chips.

Kvamme et al. [US 6,175,883 B1] disclose system for increasing data transfer rate using synchronous DMA transfer protocol by reducing a timing delay at both sending and receiving devices.

Bhattacharya [US 5,918,072 A] discloses system for controlling variable length PCI burst data using a dummy final data phase and adjusting the burst length during transaction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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